CLAIMS

1. (original) A method for manufacturing a semiconductor device, comprising steps of:

forming source and drain extension regions in an upper surface of a SiGe-based substrate, the source and drain extension regions containing an N type impurity; and

reducing vacancy concentration in the source and drain extension regions to decrease diffusion of the N type impurity contained in the first source and drain regions.

2. (original) The method of claim 1, wherein the step of reducing vacancy concentration comprises a step of providing an interstitial element or a vacancy-trapping element in the source and drain extension regions.

3. (original) The method of claim 2, wherein the interstitial element is Si or O, and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.

4. (original) The method of claim 2, wherein the step of providing the interstitial element or vacancy-trapping element comprises a step of ion-implanting the interstitial element or the vacancy-trapping element onto the SiGe-based substrate.

5. (original) The method of claim 4, wherein the step of ion-implanting the interstitial element or the vacancy trapping element comprises a step of ion-implanting the interstitial element or the vacancy trapping element at an implantation concentration of approximately 1 x 1014 atoms/cm2 to 1 x 1016 atoms/cm2 and at an implantation energy of approximately 0.3 KeV to 100 KeV.

6. (original) The method of claim 5, wherein the SiGe substrate comprises a Si cap layer on a SiGe film on a silicon substrate.

7. (original) The method of claim 6, wherein a concentration peak of the interstitial element or the vacancy-trapping element and a concentration peak of the N type impurity in the source and drain extension regions are formed at substantially the same depth from an upper surface of the Si cap layer.

8. (original) The method of claim 7, wherein the concentration peak of the interstitial element or the vacancy-trapping element is formed at a depth of approximately 10 Å to 20000 Å from the upper surface of the Si cap layer.

9. (original) The method of claim 4, further comprising a step of annealing.

10. (original) The method of claim 9, wherein the step of annealing is performed at a temperature of approximately 700° C to 1200 ° C for approximately 1 second to 3 minutes.

11. (original) The method of claim 1, further comprising a step of forming a gate electrode on the upper surface of the SiGe-based substrate with a gate oxide film therebetween.

12. (original) The method of claim 1, further comprising a step of forming source and drain regions in the upper surface of the SiGe-based substrate, the source and drain regions containing the N type impurity and overlapping the source and drain extension regions.

13. (original) The method of claim 12, further comprising a step of providing an interstitial element or a vacancy-trapping element in the source and drain regions.

14. (original) The method of claim 13, wherein the interstitial element is Si or O, and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.

15. (original) The method of claim 14, wherein the step of reducing the vacancy concentration in the source and drain regions comprises a step of ion-implanting the interstitial element or the vacancy-trapping element.

16. (original) A method for reducing diffusion of an N type impurity in a SiGe-based substrate, the method comprising steps of:

forming source and drain extension regions in an upper surface of the SiGe-based substrate; and

ion implanting an interstitial element or a vacancy-trapping element into the source and drain extension regions to reduce vacancy concentration in the source and drain extension regions.

17. (original) The method of claim 19, wherein the interstitial element is Si or O, and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.

18. (original) The method of claim 16, further comprising a step of forming source and drain regions.

19-20. (Cancelled)